We claim:

1. A method of fabricating an electronic component having semiconductor chips stacked on one another and connected via rewiring planes and through contacts formed at sawn edges of the semiconductor chip, the method which comprises the following steps:

providing a semiconductor wafer with semiconductor chips arranged in rows and columns and sawing track regions therebetween;

applying an insulating layer for protection and for insulation of an active top side of the semiconductor chips;

forming through contact holes in the sawing track regions, the contact holes having a diameter greater than a width of a saw blade for dicing the semiconductor wafer;

coating an inner wall of the through contact holes with at least one of an adhesion promoter and a solderable surface coating;

filling the through contact holes with solder material to form through contacts;

patterning the insulating layer by uncovering contact areas on the active top side of the semiconductor chip and applying interconnects for rewiring on the insulating layer, the

interconnects for rewiring connecting individual contact areas to the through contacts;

dicing the semiconductor wafer to form semiconductor chips; and

stacking a plurality of semiconductor chips to form an electronic component.

2. The method according to claim 1, wherein the step of forming the through contact holes comprises reactive ion beam etching.

3. The method according to claim 1, wherein the step of forming the through contact holes comprises laser beam vaporization.

4. The method according to claim 1, wherein the step of forming the through contact holes comprises electrolytic cannula etching.

5. The method according to claim 1, which comprises coating the inner walls of the through contact holes with an adhesion promoter selected from the group consisting of titanium and a titanium alloy.

6. The method according to claim 1, which comprises coating the inner walls of the through contact holes with a solderable surface coating selected from the group consisting of copper, silver, gold, and alloys thereof.

7. The method according to claim 1, which comprises coating the inner walls of the through contact holes with a vapor deposition process.

8. The method according to claim 7, which comprises coating the inner walls of the through contact holes with a vapor deposition process selected from the group consisting of chemical vapor deposition and physical vapor deposition.

9. The method according to claim 1, which comprises electroplating the inner walls of the through contact holes.

10. The method according to claim 1, which comprises screen printing the interconnects for rewiring on the patterned insulating layer.

11. The method according to claim 1, which comprises forming a wafer with semiconductor chips to be used as bottommost semiconductor chips of a stack, and forming solder deposits instead of through contacts on the semiconductor wafer of the bottommost semiconductor chips.

12. The method according to claim 1, which comprises stacking a plurality of semiconductor wafers on one another, connecting the through contacts to the interconnects of respectively overlying or underlying semiconductor wafers, and subsequently separating the stacked semiconductor wafers to form stacks of semiconductor chips.

13. The method according to claim 12, wherein the connecting step comprises heating the stacked semiconductor wafers to a soldering temperature.